a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node.

15. (Amended) An array as set forth in claim 12, wherein said semiconductor device comprises a field effect transistor.

16. (Amended) An array as set forth in claim 15, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer.

26. (Amended) A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:

a metal conductor; and

a conductive via comprising a diffusion barrier material formed on said metal conductor;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer; and

a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by said conductive via.

32. (Amended) The array according to claim 26, further comprising:

a plurality of field effect transistors, each node in said plurality of semiconductor nodes forming a part of each field effect transistor.